

WE CLAIM:

1 1. A multithreaded processor, comprising:
2 a fetch control unit, having an input coupled to receive an execution feedback
3 signal with information related to a plurality of threads on a per thread
4 basis, the fetch control unit generating an instruction fetch sequence based
5 on the execution feedback signal; and
6 an instruction cache, having an input coupled to an output of the fetch control
7 unit, the instruction cache dispatching instruction data responsive to the
8 instruction fetch sequence.

1 2. The multithreaded processor of claim 1, further comprising an
2 instruction queue having an output coupled to the fetch control unit input, the instruction
3 queue generating a queue feedback signal responsive to a thread queue condition associated
4 with a thread from the plurality of threads, wherein the fetch control unit generates the
5 instruction fetch sequence also based on the queue feedback signal.

1 3. The multithreaded processor of claim 2, wherein the thread queue
2 condition indicates that a thread queue has less than a first amount of remaining storage.

1 4. The multithreaded processor of claim 2, wherein the thread queue
2 condition indicates that a thread queue has less than a second amount of remaining decoded
3 instructions.

1 5. The multithreaded processor of claim 1, wherein the fetch control unit
2 blocks the thread from the instruction fetch sequence responsive to the queue feedback
3 signal.

1 6. The multithreaded processor of claim 1, wherein the fetch control unit
2 advances the thread in the instruction fetch sequence responsive to the queue feedback signal.

1 7. The multithreaded processor of claim 1, further comprising a thread
2 interleaver having an output coupled to the fetch control unit input, the thread interleaver

3 generating an interleaver feedback signal responsive to a thread condition, wherein the fetch
4 control unit generates the instruction fetch sequence also based on the interleaver feedback
5 signal.

1 8. The multithreaded processor of claim 1, wherein the thread condition
2 indicates that a thread from the plurality of threads is ineligible for execution.

1 9. The multithreaded processor of claim 1, wherein the thread interleaver
2 generates a thread execution sequence independent of the instruction fetch sequence.

1 10. The multithreaded processor of claim 1, further comprising an
2 execution pipeline having an output coupled to the fetch control unit input, the execution
3 pipeline generating the execution feedback signal responsive to an execution stall.

1 11. The multithreaded processor of claim 1, wherein the fetch control unit
2 delays the thread in the instruction fetch sequence responsive to the execution stall.

1 12. The multithreaded processor of claim 1, wherein the execution stall
2 comprises one from the group consisting of a branch misprediction, an exception, a data
3 cache miss, an external resource stall, an interlock, and a memory operation ordering.

1 13. The multithreaded processor of claim 1, wherein the fetch control unit
2 generates the instruction fetch sequence, in a default state, by selecting a thread from the
3 plurality of threads according to round robin arbitration.

1 14. The multithreaded processor of claim 1, wherein the execution
2 feedback signal is capable of including information related to each of the plurality of threads.

1 15. The multithreaded processor of claim 1, wherein the multithreaded
2 processor is a multithreaded network processor and the instruction data are packet processing
3 instructions related to at least one from the group consisting of: packet routing, switching,
4 bridging and forwarding.

1 16. A multithreaded processor, comprising:
2 means for fetching, having an input coupled to receive an execution feedback
3 signal with information related to a plurality of threads on a per thread
4 basis, the means for fetching generating an instruction fetch sequence
5 based on the execution feedback signal; and
6 means for storing, having an input coupled to an output of the means for fetching,
7 the means for storing dispatching instruction data responsive to the
8 instruction fetch sequence.

1 17. The multithreaded processor of claim 16, further comprising a means
2 for queuing having an output coupled to the means for fetching input, the means for queuing
3 generating a queue feedback signal responsive to a thread queue condition associated with a
4 thread from the plurality of threads, wherein the means for fetching generates the instruction
5 fetch sequence also based on the queue feedback signal.

1 18. The multithreaded processor of claim 17, wherein the thread queue
2 condition indicates that a means for thread queuing has less than a first amount of remaining
3 storage.

1 19. The multithreaded processor of claim 17, wherein the thread queue
2 condition indicates that a means for thread queuing has less than a second amount of
3 remaining decoded instructions.

1 20. The multithreaded processor of claim 16, wherein the means for
2 fetching blocks the thread from the instruction fetch sequence responsive to the queue
3 feedback signal.

1 21. The multithreaded processor of claim 20, wherein the means for
2 fetching advances the thread in the instruction fetch sequence responsive to the queue
3 feedback signal.

1 22. The multithreaded processor of claim 16, further comprising a means
2 for interleaving having an output coupled to the means for fetching input, the means for
3 interleaving generating an interleaver feedback signal responsive to a thread condition,
4 wherein the means for fetching generates the instruction fetch sequence also based on the
5 interleaver feedback signal.

1 23. The multithreaded processor of claim 16, wherein the thread condition
2 indicates that a thread from the plurality of threads is ineligible for execution.

1 24. The multithreaded processor of claim 16, wherein the means for
2 interleaving generates a thread execution sequence independent of the instruction fetch
3 sequence.

1 25. The multithreaded processor of claim 16, further comprising an means
2 for executing having an output coupled to the means for fetching input, the means for
3 executing generating the execution feedback signal responsive to an execution stall.

1 26. The multithreaded processor of claim 16, wherein the means for
2 fetching delays the thread in the instruction fetch sequence responsive to the execution stall.

1 27. The multithreaded processor of claim 16, wherein the execution stall
2 comprises one from the group consisting of a branch misprediction, an exception, a data
3 cache miss, an external resource stall, an interlock, and a memory operation ordering.

1 28. The multithreaded processor of claim 16, wherein the means for
2 fetching generates the instruction fetch sequence, in a default state, by selecting a thread from
3 the plurality of threads according to round robin arbitration.

1 29. The multithreaded processor of claim 16, wherein the execution
2 feedback signal is capable of including information related to each of the plurality of threads.

1 30. The multithreaded processor of claim 16, wherein the multithreaded
2 processor is a multithreaded network processor and the instruction data are packet processing

3 instructions related to at least one from the group consisting of: packet routing, switching,
4 bridging and forwarding.

1 31. A method for fetching instructions in a multithreaded processor,
2 comprising:
3 generating an instruction fetch sequence based on an execution feedback signal
4 with information related to a plurality of threads on a per thread basis; and
5 dispatching instruction data responsive to the instruction fetch sequence.

1 32. The method of claim 31, further comprising
2 generating a queue feedback signal responsive to a thread queue condition
3 associated with a thread from the plurality of threads.

1 33. The method of claim 32, wherein the thread queue condition indicates
2 that a thread queue has less than a first amount of remaining storage.

1 34. The method of claim 32, wherein the thread queue condition indicates
2 that a thread queue has less than a second amount of remaining decoded instructions.

1 35. The method of claim 31, wherein the generating the instruction fetch
2 sequence comprises blocking the thread from the instruction fetch sequence responsive to the
3 queue feedback signal.

1 36. The method of claim 35, wherein the generating the instruction fetch
2 sequence comprises advancing the thread in the instruction fetch sequence responsive to the
3 queue feedback signal.

1 37. The method of claim 31, wherein the generating the instruction fetch
2 sequence further comprises generating an interleaver feedback signal responsive to a thread
3 condition in a thread interleaver.

1 38. The method of claim 31, wherein the thread condition indicates that a
2 thread from the plurality of threads is ineligible for execution.

1 39. The method of claim 31, wherein the generating the feedback signal
2 comprises generating a thread execution sequence independent of the instruction fetch
3 sequence.

1 40. The method of claim 31, the generating the instruction fetch sequence
2 further comprises generating the execution feedback signal responsive to an execution stall.

1 41. The method of claim 31, wherein the generating the instruction fetch
2 sequence further comprises delaying the thread in the instruction fetch sequence responsive
3 to the execution stall.

1 42. The method of claim 31, wherein the execution stall comprises one
2 from the group consisting of a data cache miss, an external resource stall, an interlock, and a
3 memory operation ordering.

1 43. The method of claim 31, wherein the generating the instruction fetch
2 sequence comprises generating the instruction fetch sequence, in a default state, by selecting
3 a thread from the plurality of threads according to round robin arbitration.

1 44. The method of claim 31, wherein the feedback signal is capable of
2 including information related to each of the plurality of threads.

1 45. The method of claim 31, wherein the multithreaded processor is a
2 multithreaded network processor and the instruction data are packet processing instructions
3 related to at least one form the group consisting of: packet routing, switching, bridging and
4 forwarding.